Abstracts

Language design requirements for VHDL-RF/MW/sup TM/

This paper describes design requirements for VHDL-RF/MW/sup TM/. The resulting language design addresses distributed and full-wave interconnect models, frequency-domain modeling and parasitic interactions so as to maintain full conceptual and representational compatibility with VHDL, VHDL-AMS, Verilog, Verilog-AMS and SPICE.

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